Research Associate for Design and Verification of RISC-V Systems and HPC Accelerators (m/f/d)

Technische Fakultät, Erlangen, TV-L E 13, Vollzeit, Befristete Anstellung: bis 31.12.2027, Bewerbungsschluss: 10.09.2025

Your Workplace

The Institute of System-on-Chip Design at the Faculty of Engineering of Friedrich-Alexander-University Erlangen-Nürnberg (FAU) specializes in the design of digital circuits and is one of the leading institutions in this field. Here, innovative approaches and methods are developed to create efficient and high-performance digital integrated circuits (ICs). The institute places great emphasis on practical research and promotes collaboration with industry to ensure the transfer of knowledge and technologies. The close cooperation with the Fraunhofer Institute for Integrated Circuits (IIS) provides doctoral candidates with unique opportunities to extend their research activities beyond the purely academic context and gain practical experience in industry. With modern laboratories and highly qualified professionals, the institute provides optimal conditions for students and researchers to develop cutting-edge solutions in the field of digital circuit technologies. The position will be within the framework of the Bavarian Chip Design Center (BCDC).

Benefits: We Have a Lot To Offer

- Regular promotion to the next level and increase in salary pursuant to the collective bargaining agreement for the public service of the German Länder (TV-L) or remuneration pursuant to the Bavarian Public Servants Remuneration Act (BayBesG) plus an additional annual bonus
- 30 days annual leave at five working days per week with additional free days on December 24 and 31
- Occupational pension scheme and asset accumulation savings scheme

Your Tasks

- Integrated hardware accelerators for machine learning in RISC-V subsystems
- Hardware and hardware-related software for methods and strategies for battery-powered IoT nodes with an optimized RISC-V processor subsystem for ultra-low power consumption
- Hard- and software co-optimized architectures and strategies for high-performance, energy-efficient hardware accelerators, as well as a System-on-Chip with a RISC-V
- Methods and strategies for efficient functional and formal digital verification, including the emulation of digital System-on-Chip (SoC) with RISC-V and mixed-signal IPs
- Expansion of collaboration with the Fraunhofer IIS and other institutes in the field
- Publication and presentation of research results
- Supervision of Bachelor's and Master's theses, as well as conducting teaching exercises,

seminars, or computer labs

Your Profile

- Completed academic degree (Master's/Diploma) in digital circuit technology or a related field
- The duties require you to comply with US Export Restrictions (EAR) --> https://www.bis.gov/regulations/ear
- Good knowledge of SystemVerilog and/or VHDL
- Knowledge about FPGA design flows as well as ASIC design flows from RTL to GDS
- Excellent English skills

Interessiert?

Die vollständige Stellenausschreibung sowie alle Infos zum Bewerbungsverfahren finden Sie hier: